TFT LCD Preliminary Specification

MODEL NO.: N141C3 - L07

Customer:	Lenovo
Approved by:	
Note:	

記錄	工作	審核	角色	投票
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REVISION HISTORY

Version	Date	Page (New)	Section	Description
1.1	May 12, 08'	All	All	Preliminary specification was first issued.
		15	5.5	Update EDID Data

1 GENERAL DESCRIPTION

1.1 OVERVIEW

N141C3 - L07 is a 14.1" TFT Liquid Crystal Display module with single CCFL Backlight unit and 30 pins LVDS interface. This module supports 1440 x (3 BGR) x 900 WXGA+ mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction. The inverter module for backlight is not built in.

1.2 FEATURES

- Thin and Light Weight
- WXGA+ (1440 x 900 pixels) resolution
- DE only mode
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 2 pixel/clock
- RoHS compliance

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	303.48(H) X 189.675(V) (14.1 inch Diagonal)	mm	(1)
Bezel Opening Area	306.76 (H) x 193.0 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1440 x B.G.R. x 900	pixel	-
Pixel Pitch	0.21075 (H) x 0.21075 (V)	mm	-
Pixel Arrangement	BGR vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Anti-glare and Hard Coat (3H min.)	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	319	319.5	320	mm	(1)
	Vertical(V)	205	205.5	206	mm	
	Depth(D)	--	5.2	5.5	mm	
Weight		--	400	415	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions

2 ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

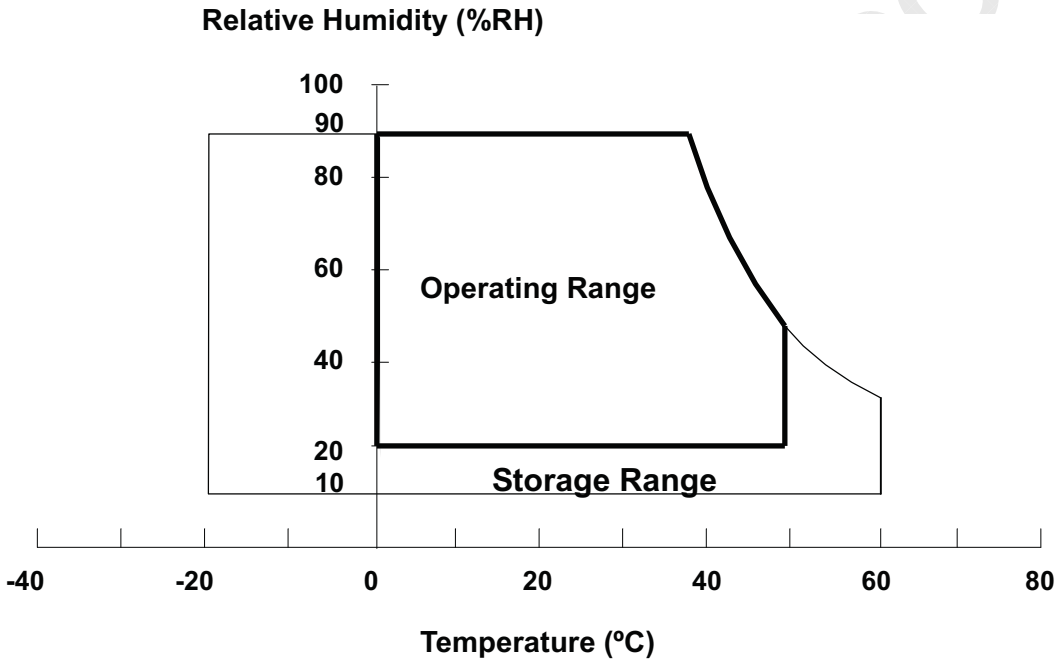
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	220/2	G/ms	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.5	G	(4), (5)

Note (1) (a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The temperature of panel display surface area should be 0 ºC Min. and 60 ºC Max..

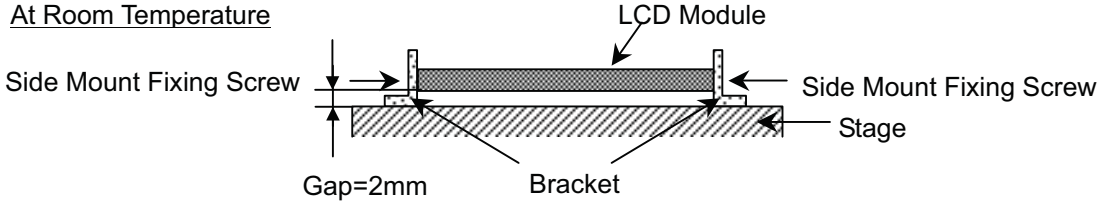


Note (3) 1 time for ± X, ± Y, ± Z. for Condition (220G / 2ms) is half Sine Wave,.

Note (4) 10 ~ 500 Hz, 30 min / Cycle, 1 cycles for each X, Y, Z axis.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	V_{CC}+0.3	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_L	-	2.5K	V_{RMS}	(1), (2)
Lamp Current	I_L	2.0	6.5	mA_{RMS}	(1), (2)
Lamp Frequency	F_L	45	80	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 3.2 for further information).

3 ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

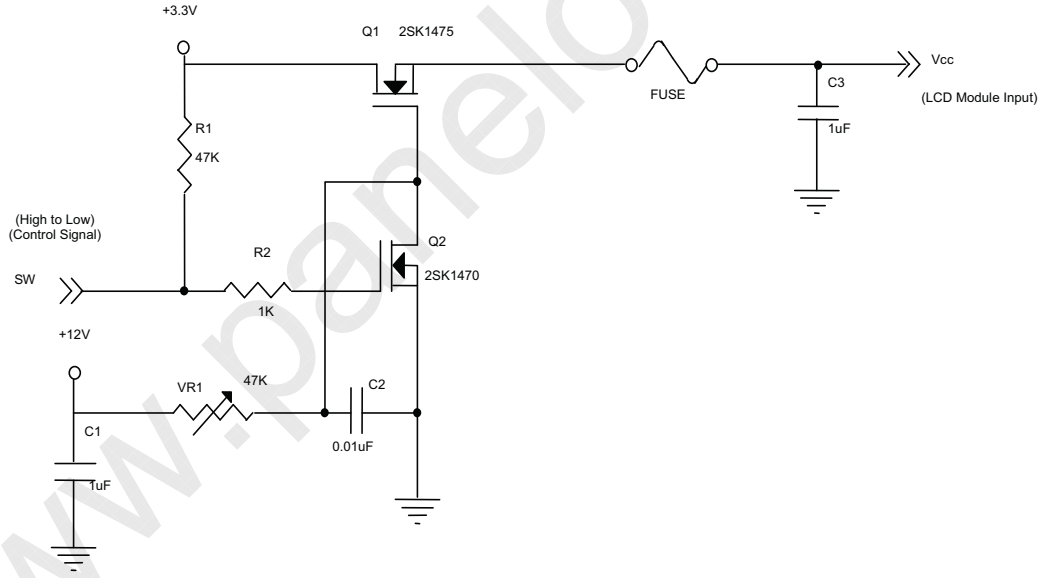
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	3.0	3.3	3.6	V	-
Permissive Ripple Voltage		V_{RP}	-	50	-	mV	-
Rush Current		I_{RUSH}	-	-	1.5	A	(2)
Initial Stage Current		I_{IS}	-	-	1.0	A	(2)
Power Supply Current	White	Icc	-	360	-	mA	(3)a
	Black		-	450	-	mA	(3)b
LVDS Differential Input High Threshold		$V_{TH(LVDS)}$	-	-	+100	mV	(5), V_{CM}=1.2V
LVDS Differential Input Low Threshold		$V_{TL(LVDS)}$	-100	-	-	mV	(5) V_{CM}=1.2V
LVDS Common Mode Voltage		V_{CM}	1.125	-	1.375	V	(5)
LVDS Differential Input Voltage		$\|V_{ID}\|$	100	-	600	mV	(5)
Terminating Resistor		R_T	-	100	-	Ohm	-
Power per EBL WG		P_{EBL}	-	3.54	-	W	(4)

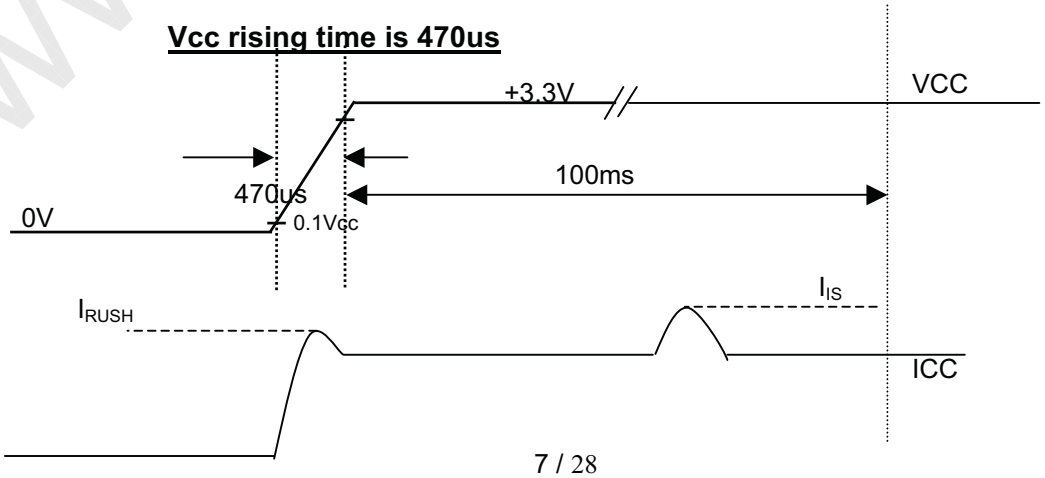
Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) I_{RUSH}: the maximum current when VCC is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.





Note (3) The specified power supply current is under the conditions at Vcc = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

Active Area

b. Black Pattern

Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.

(a) Vcc = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz,

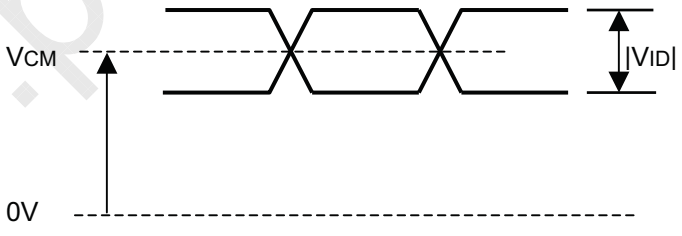
(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

(c) Luminance: 60 nits.

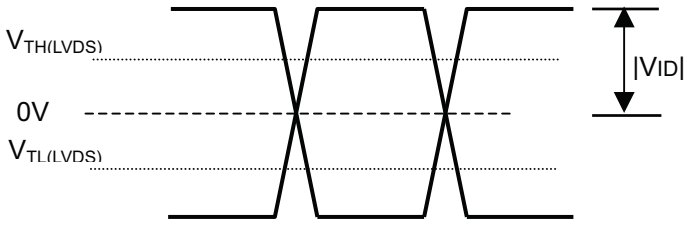
(d) The inverter used is provided from Sumida. Please contact them for detail information. CMO doesn't provide the inverter in this product.

Note (5) The parameters of LVDS signals are defined as the following figures.

Single Ended



Differential

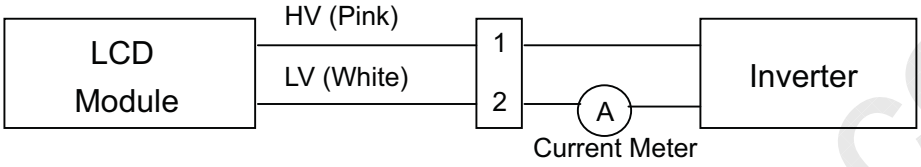


3.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	612	680	748	V_{RMS}	I_L = 6.0 mA
Lamp Current	I_L	2.0	6.0	6.5	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	-	-	1370 (25 °C)	V_{RMS}	(2)
		-	-	1520 (0 °C)	V_{RMS}	(2)
Operating Frequency	F_L	45	-	80	KHz	(3)
Lamp Life Time	L_{BL}	15,000	-	-	Hrs	(5)
Power Consumption	P_L	-	4.08	-	W	(4), I_L = 6.0 mA

Note (1) Lamp current is measured by utilizing a high frequency current meter as shown below:



Note (2) The voltage that must be larger than Vs should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) $P_L = I_L \times V_L$

Note (5) The lifetime of lamp can be defined as the time in which it continues to operate under the condition Ta = 25 ±2 °C and I_L = 6 mArms until one of the following events occurs:

(a) When the brightness becomes or lower than 50% of its original value.

(b) When the effective ignition length becomes or lower than 80% of its original value.

(The effective ignition length is a scope that luminance is over 70% of that at the center point.)

Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid producing too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform.(Unsymmetrical ratio is less than 10%) Please do not use the inverter which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may

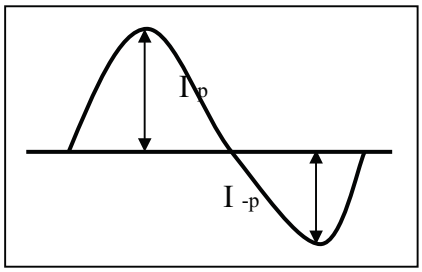
produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

a. The asymmetry rate of the inverter waveform should be 10% below.

b. The distortion rate of the waveform should be within √2 ± 10%.

c. The ideal sine wave form shall be symmetric in positive and negative polarities.



* Asymmetry rate:

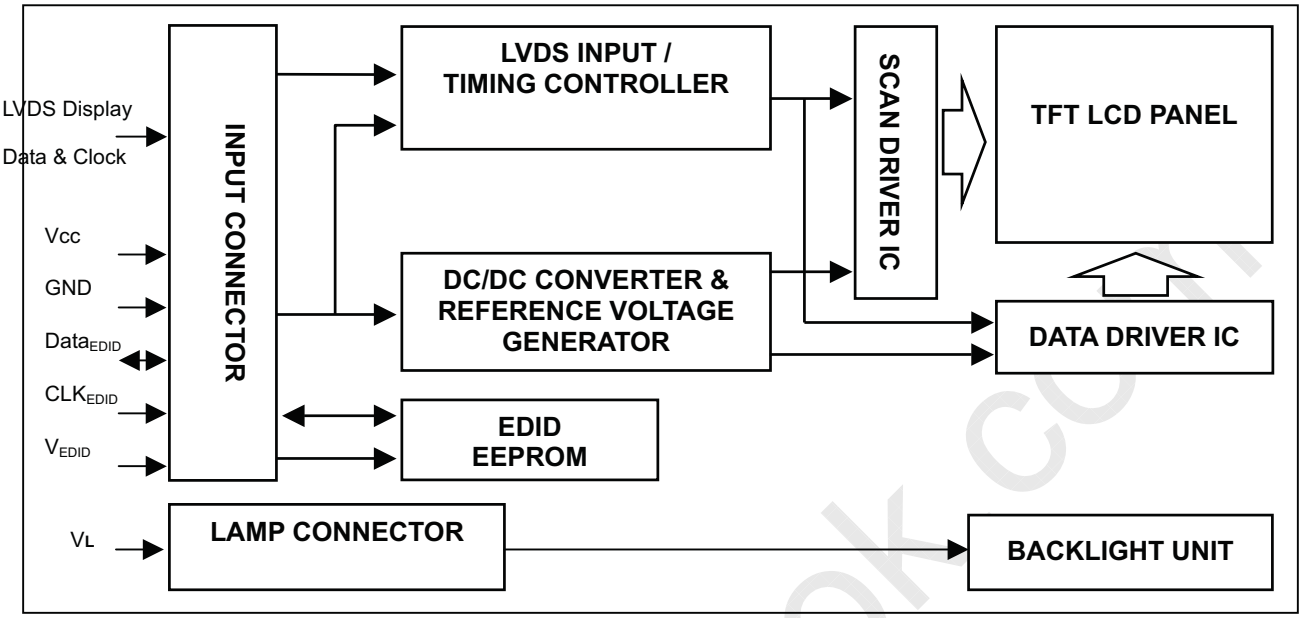
$| I_p - I_{-p} | / I_{rms} * 100\%$

* Distortion rate

I_p (or I_{-p}) / I_{rms}

4 BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT

5 INPUT TERMINAL PIN ASSIGNMENT

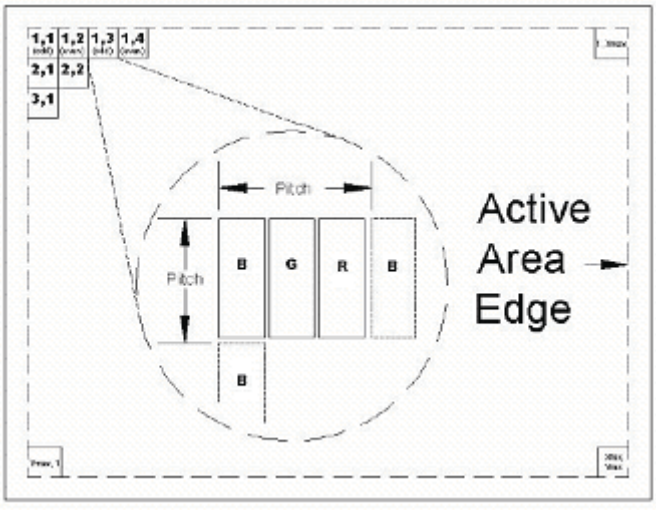
5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Vss	Ground		
2	Vcc	Power Supply +3.3 V (typical)		
3	Vcc	Power Supply +3.3 V (typical)		
4	V_{EDID}	DDC 3.3V Power		
5	NC	Non-Connection		
6	CLK_{EDID}	DDC Clock		
7	$DATA_{EDID}$	DDC Data		-
8	RXO0-	LVDS Differential Data Input (Odd)	Negative	
9	RXO0+	LVDS Differential Data Input (Odd)	Positive	
10	Vss	Ground		
11	RXO1-	LVDS Differential Data Input (Odd)	Negative	
12	RXO1+	LVDS Differential Data Input (Odd)	Positive	
13	Vss	Ground		
14	RXO2-	LVDS Differential Data Input (Odd)	Negative	
15	RXO2+	LVDS Differential Data Input (Odd)	Positive	
16	Vss	Ground		
17	RXOC-	LVDS Clock Data Input (Odd)	Negative	
18	RXOC+	LVDS Clock Data Input (Odd)	Positive	
19	Vss	Ground		
20	RxE0-	LVDS Differential Data Input (Even)	Negative	
21	RxE0+	LVDS Differential Data Input (Even)	Positive	
22	Vss	Ground		
23	RxE1-	LVDS Differential Data Input (Even)	Negative	
24	RxE1+	LVDS Differential Data Input (Even)	Positive	
25	Vss	Ground		
26	RxE2-	LVDS Differential Data Input (Even)	Negative	
27	RxE2+	LVDS Differential Data Input (Even)	Positive	
28	Vss	Ground		
29	RXEC-	LVDS Clock Data Input (Even)	Negative	
30	RXEC+	LVDS Clock Data Input (Even)	Positive	

Note (1) Connector Part No.: JAE-FI-XB30SRL-HF11 or equivalent

Note (2) User's connector Part No: JAE-FI-X30C2L or equivalent

Note (3) The first pixel is odd as shown in the following figure.



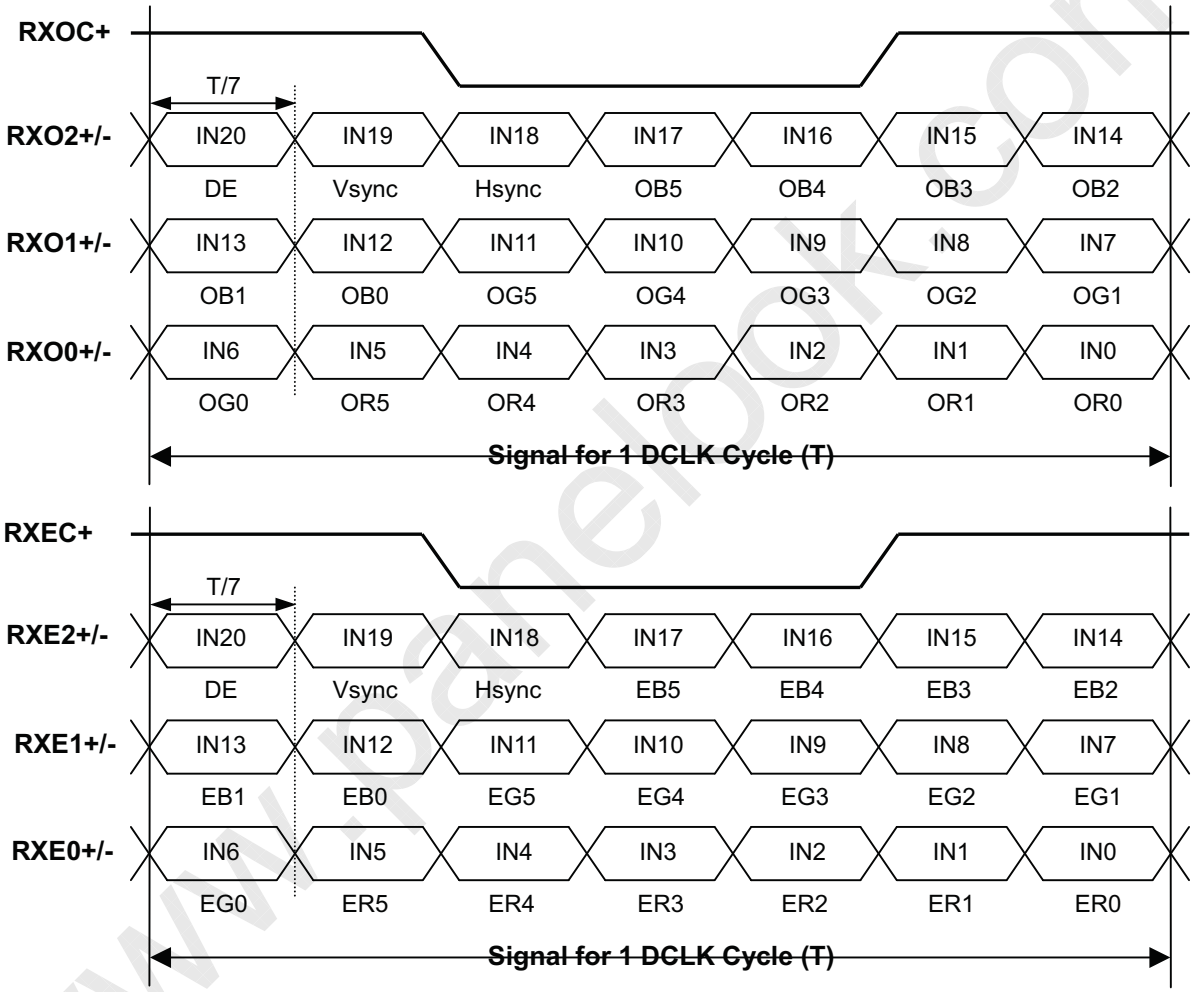
5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Color
1	HV	High Voltage	Pink
2	LV	Ground	White

Note (1) Connector Part No.: JST- BHSR-02VS-1 or equivalent

Note (2) User's connector Part No.: SM02B-BHSS-1-TB or equivalent

5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL



5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.5 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header , Fixed	00	00000000
1	1	Header , Fixed	FF	11111111
2	2	Header , Fixed	FF	11111111
3	3	Header , Fixed	FF	11111111
4	4	Header , Fixed	FF	11111111
5	5	Header , Fixed	FF	11111111
6	6	Header , Fixed	FF	11111111
7	7	Header , Fixed	00	00000000
8	8	ID=Lenovo	30	00110000
9	9	ID=Lenovo	AE	10101110
10	0A	XGA (Lenovo Unique ID)	33	00110011
11	0B	XGA (Lenovo Unique ID)	40	01000000
12	0C	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
13	0D	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
14	0E	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
15	0F	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
16	10	Week of manufacture 1 - 53 (unused: 00h)	14	00010100
17	11	Year of manufacture year - 1990(unsed:00h)	12	00010010
18	12	Version=1	01	00000001
19	13	Revision=3	03	00000011
20	14	Digital	80	10000000
21	15	Active area horizontal 30.348cm	1E	00011110
22	16	Active area vertical 18.9675cm	13	00010011
23	17	gamma * 100-100 = 2.2*100-100=120	78	01111000
24	18	Feature support (no DPMS, Active off, RGB, Preferred Timing Mode)	EA	11101010
25	19	Rx1 Rx0 Ry1 Ry0 Gx1 Gx0 Gy1 Gy0	87	10000111
26	1A	Bx1 Bx0 By1 By0 Wx1 Wx0 Wy1 Wy0	F5	11110101
27	1B	Rx=0.58	94	10010100
28	1C	Ry=0.34	57	01010111
29	1D	Gx=0.31	4F	01001111
30	1E	Gy=0.55	8C	10001100
31	1F	Bx=0.155	27	00100111
32	20	By=0.155	27	00100111
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2 (1440x900@60Hz)	00	00000000
37	25	No manufacturer's specific timing	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001
42	2A	Standard timing ID # 3	01	00000001

43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock (“96.5MHz”, According to VESA CVT Rev1.1)	B2	10110010
55	37	96.5MHz/10000 =9650=25B2H	25	00100101
56	38	HActive(D7-D0) = 1440 mod 256	A0	10100000
57	39	HBlank(D7-D0) = 266 mod 256	0A	00001010
58	3A	HActive(D11-D8) : HBlank(D11-D8) = 1440/256 : 266/256	51	01010001
59	3B	VActive(D7-D0) = 900 mod 256	84	10000100
60	3C	VBlank(D7-D0) = 43 mod 256	2B	00101011
61	3D	VActive(D11-D8) : VBlank(D11-D8) = 900/256 : 43/256	30	00110000
62	3E	HSyncOffset(D7-D0) = HBorder+HFrontPorch = 82	52	01010010
63	3F	HSyncWidth(D7-D0) = 54	36	00110110
64	40	VSyncOffset(D3-D0)=5 : VSyncWidth(D3-D0)=9	59	01011001
65	41	HSyncOffset(D9-D8) : HSyncWidth(D9-D8) : VSyncOffset(D5-D4) : VSyncWidth(D5-D4)	00	00000000
66	42	HImageSize(mm, D7-D0) = 303mod 256	2F	00101111
67	43	VImageSize(mm, D7-D0) = 190mod 256	BE	10111110
68	44	HImageSize(D11-D8) : VImageSize(D11-D8) = 303/256 : 190/256	10	00010000
69	45	Horizontal Border=0	00	00000000
70	46	Vertical Border=0	00	00000000
71	47	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	18	00011000
72	48	Detailed timing description # 1 Pixel clock (“80.44MHz”, According to VESA CVT Rev1.1)	6C	01101100
73	49	80.44MHz/10000 =8044=1F6CH	1F	00011111
74	4A	Horizontal Active =1440 mod 256	A0	10100000
75	4B	Horizontal Blanking =266 mod 256	0A	00001010
76	4C	HActive(D11-D8) : HBlank(D11-D8) = 1440/256 : 266/256	51	01010001
77	4D	Vertical Avtive =900 mod 256	84	10000100
78	4E	Vertical Blanking =43 mod 256	2B	00101011
79	4F	VActive(D11-D8) : VBlank(D11-D8) = 900/256 : 43/256	30	00110000
80	50	Horizontal Sync. Offset =82	52	01010010
81	51	Horizontal Sync Pulse Width =54	36	00110110
82	52	VSyncOffset(D3-D0)=5 : VSyncWidth(D3-D0)=9	59	01011001
83	53	Horizontal Vertical Sync Offset/Width upper 2bits = 0	00	00000000
84	54	HImageSize(mm, D7-D0) = 303mod 256	2F	00101111
85	55	VImageSize(mm, D7-D0) = 190mod 256	BE	10111110
86	56	HImageSize(D11-D8) : VImageSize(D11-D8) = 303/256 : 190/256	10	00010000

87	57	Horizontal Border=0	00	00000000
88	58	Vertical Border=0	00	00000000
89	59	Non-interlaced,Normal display,no stereo,Digital separate sync,H/V pol negatives	18	00011000
90	5A	Flag	00	00000000
91	5B	Flag	00	00000000
92	5C	Flag	00	00000000
93	5D	Data type tag :0F	0F	00001111
94	5E	Flag	00	00000000
95	5F	Low Refresh Rate #1 (Horizontal active pixels / 8) - 31=95H	95	10010101
96	60	Low Refresh Rate #1 Image Aspect ratio(16 :10)	0A	00001010
97	61	Low Refresh Rate #1 Refresh Rate=50Hz	32	00110010
98	62	Low Refresh Rate #2 (Horizontal active pixels / 8) - 31=95H	95	10010101
99	63	Low Refresh Rate #2 Image Aspect ratio(16 : 10)	0A	00001010
100	64	Low Refresh Rate #2 Refresh Rate=40Hz	28	00101000
101	65	Brightness (1/10nit) , 220/10=22(=0Fh)	16	00010110
102	66	Feature Flags	01	00000001
103	67	Reserved	00	00000000
104	68	EISA manufacturer code(3 Character ID) -CMO	0D	00001101
105	69	Compressed ASCII	AF	10101111
106	6A	Panel Supplier Reserved - Product code -1439	39	00111001
107	6B	(Hex, LSB first)	14	00010100
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000
110	6E	Flag	00	00000000
111	6F	Data type tag : FEh	FE	11111110
112	70	Flag	00	00000000
113	71	"N"	4E	01001110
114	72	"1"	31	00110001
115	73	"4"	34	00110100
116	74	"1"	31	00110001
117	75	"C"	43	01000011
118	76	"3"	33	00110011
119	77	"-"	2D	00101101
120	78	"L"	4C	01001100
121	79	"0"	30	00110000
122	7A	"7"	37	00110111
123	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
124	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
125	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
126	7E	No extension	00	00000000
127	7F	One-byte checksum of entire 128 bytes EDID equals 00h.	E9	11101001

6 INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The specifications of input signal timing are as the following table and timing diagram.

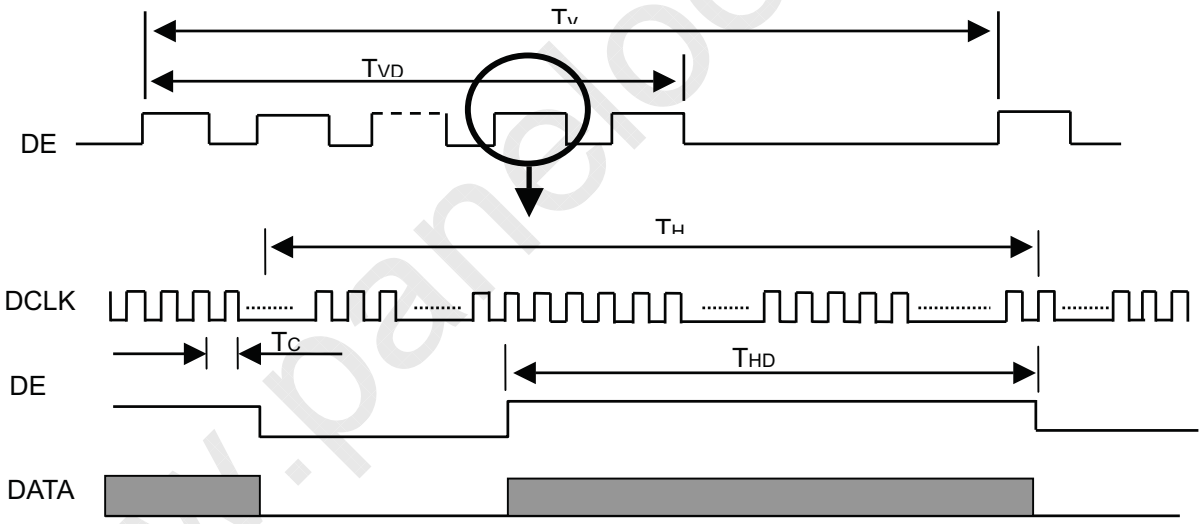
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	25	44.5	60	MHz	(2) (3)
DE	Vertical Total Time	TV	910	926	1500	TH	-
	Vertical Active Display Period	TVD	900	900	900	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	26	TV-TVD	TH	
	Horizontal Total Time	TH	760	800	880	Tc	(2)
	Horizontal Active Display Period	THD	720	720	720	Tc	(2)
	Horizontal Active Blanking Period	THB	TH-THD	80	TH-THD	Tc	(2)

Note (1) Because this module is operated by DE only mode, Hsync and Vsync are ignored.

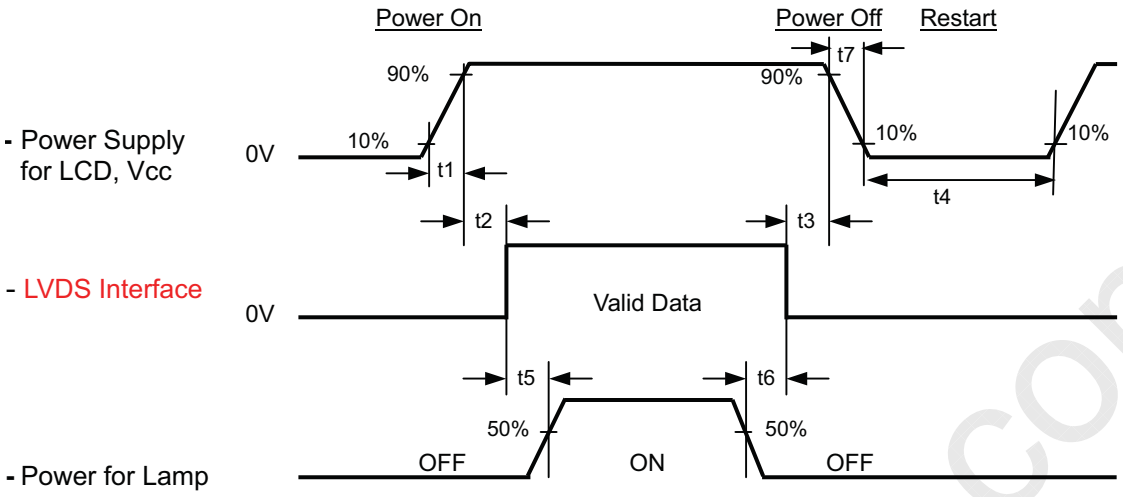
(2) 2 channels LVDS input.

(3) The module can be operated at 40Hz refresh rate. However, there might be some side effect like flicker, brightness change or etc.

INPUT SIGNAL TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE



Timing Specifications:

t1 ≦ 10 msec

0 < t2 ≦ 50 msec

0 < t3 msec

t4 ≧ 150 msec

t5 ≧ 200 msec

t6 ≧ 0 msec

t7 ≦10 msec

Note (1) Please follow the power on/off sequence described above. Otherwise, the LCD module might be damaged.

Note (2) Please avoid floating state of interface signal at invalid period. When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time is better to follow 5≦t7≦300 ms.

7 OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

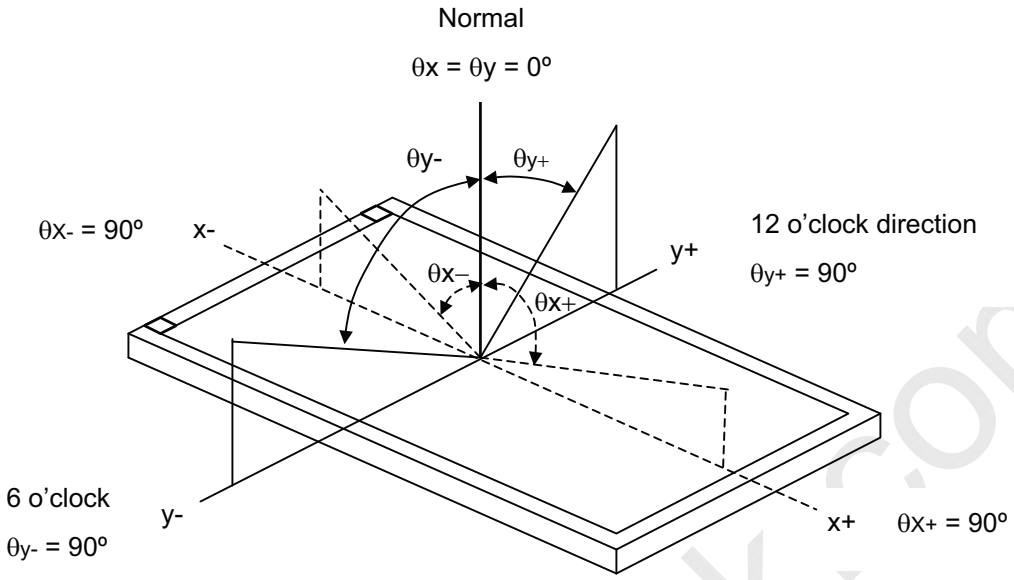
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I_L	6.0	mA
Inverter Driving Frequency	F_L	61	KHz
Inverter	Sumida H05-4915		

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

7.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	(250)	(400)	-	-	(2), (5)
Response Time		T_R		-	3	8	ms	(3)
		T_F		-	7	12	ms	
Average Luminance of White		L_{AVE}		170	200	-	cd/m^2	(4), (5)
White Variation		δW 5pts		-	-	1.4	-	(5)
Color Chromaticity	Red	Rx		TYP -0.03	(0.610)	TYP +0.03	-	(1), (5)
		Ry			(0.331)		-	
	Green	Gx			(0.298)		-	
		Gy			(0.548)		-	
	Blue	Bx			(0.160)		-	
		By			(0.156)		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	40	45	-	Deg.	
		θ_x-		40	45	-		
	Vertical	θ_Y+		15	20	-		
		θ_Y-		40	45	-		

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

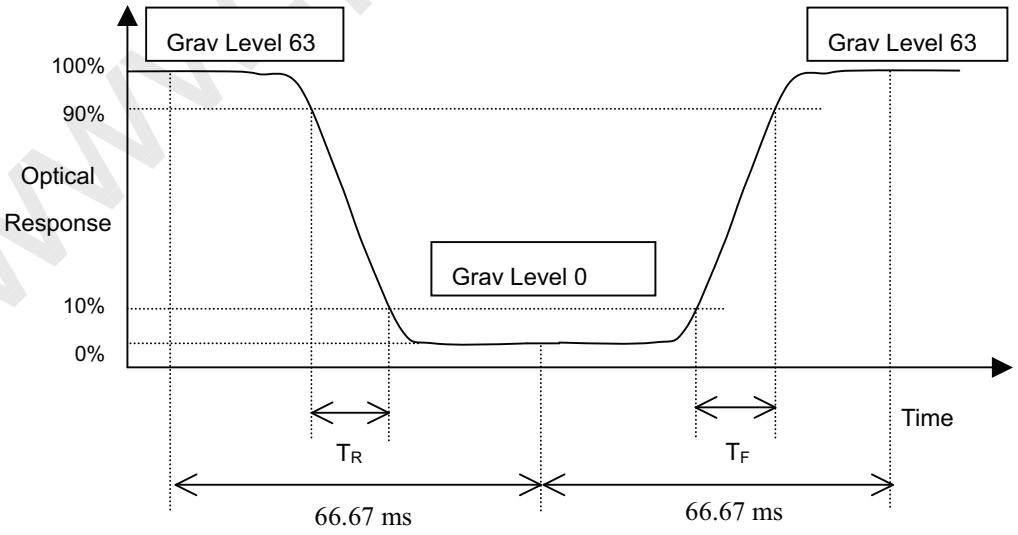
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

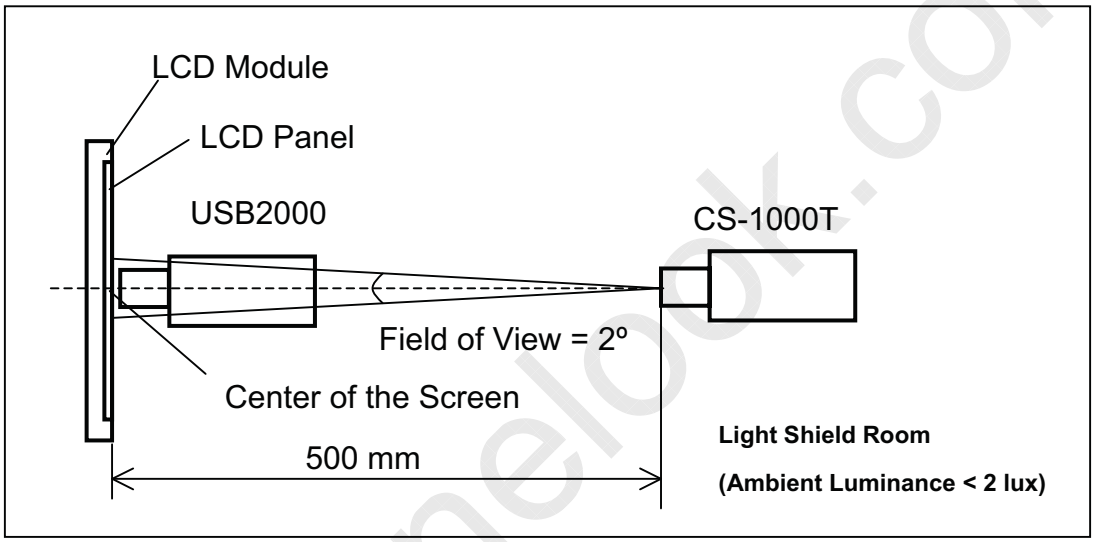
Measure the luminance of gray level 63 at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

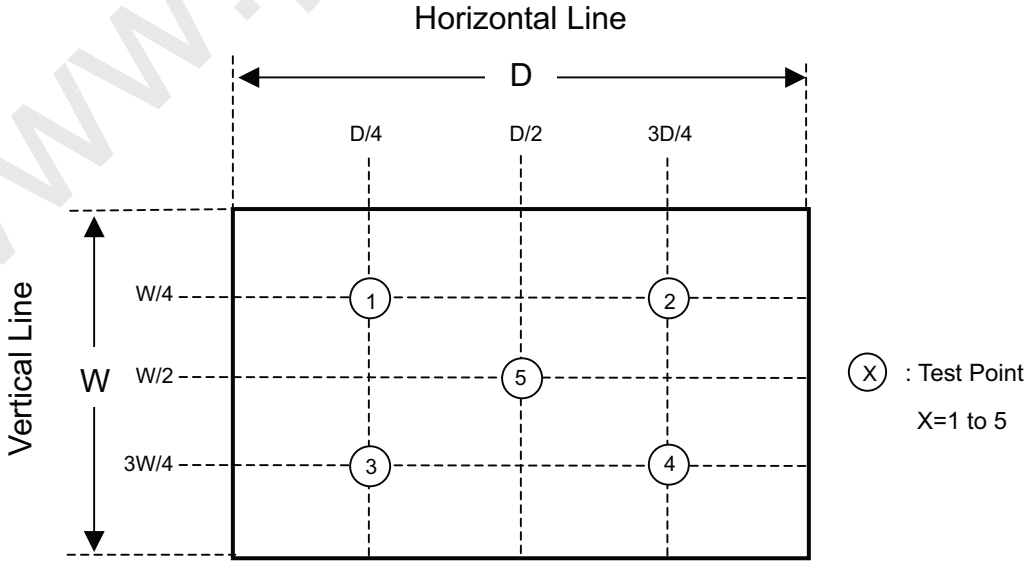
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8 PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the lamp wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

(12) To avoid wireless noise interference, please keep the antenna away from LCD control board.

8.2 SAFETY PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

9 PACKAGING

9.1 CARTON

Box Dimensions : 435(L)*350(W)*325(H)
Weight: Approx. 10.69kg(20 module .per. 1 box)

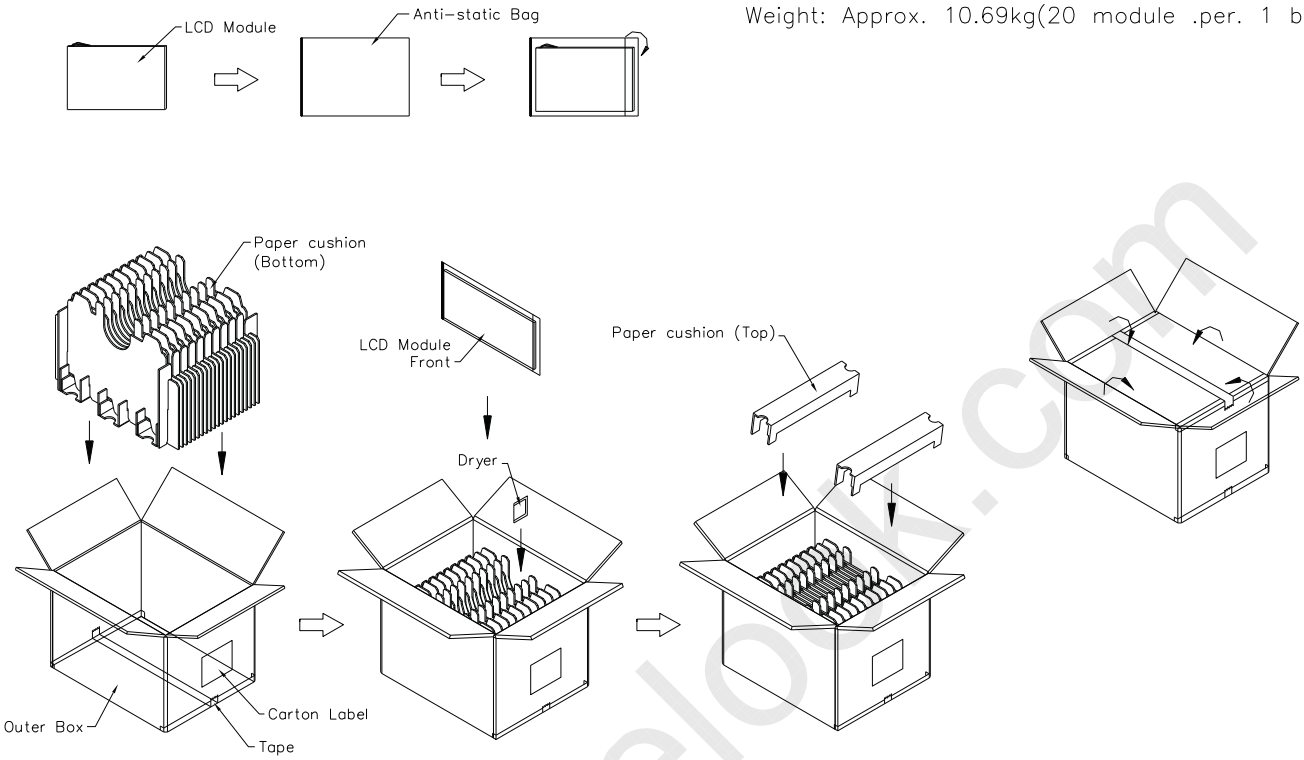


Figure. 9-1 Packing method

9.2 PALLET

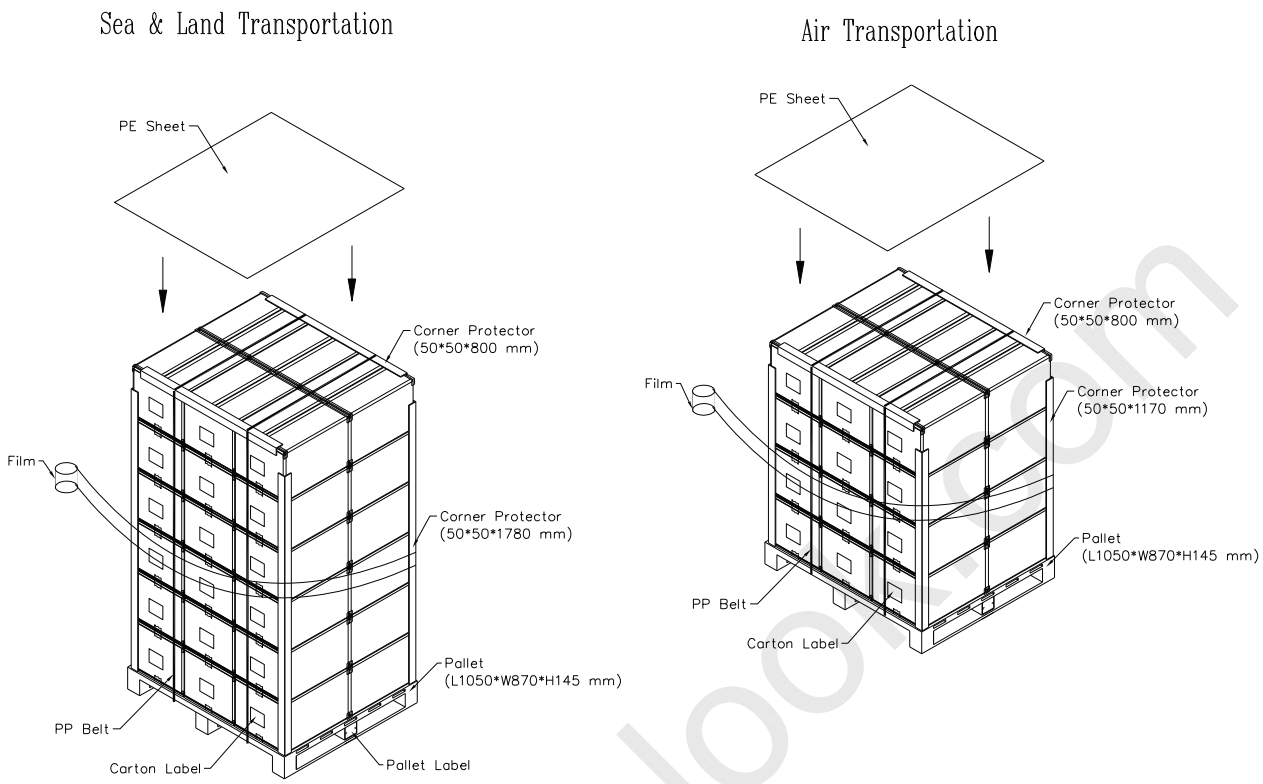


Figure. 9-2 Packing method

10 DEFINITION OF LABELS

10.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Model Name: N141C3 - L07

(b) Revision: Rev. XX, for example: A1, …, C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D X N N N N

- Serial No.
- CMO Internal Use
- Year, Month, Date
- CMO Internal Use
- Revision
- CMO Internal Use

(d) Production Location: MADE IN XXXX. XXXX stands for production location.

(e) LEOO: UL compliance remarks for CMO NingBo site production. It won't be available when production location isn't CMO NingBo.

Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

Month: 1~9, A~C, for Jan. ~ Dec.

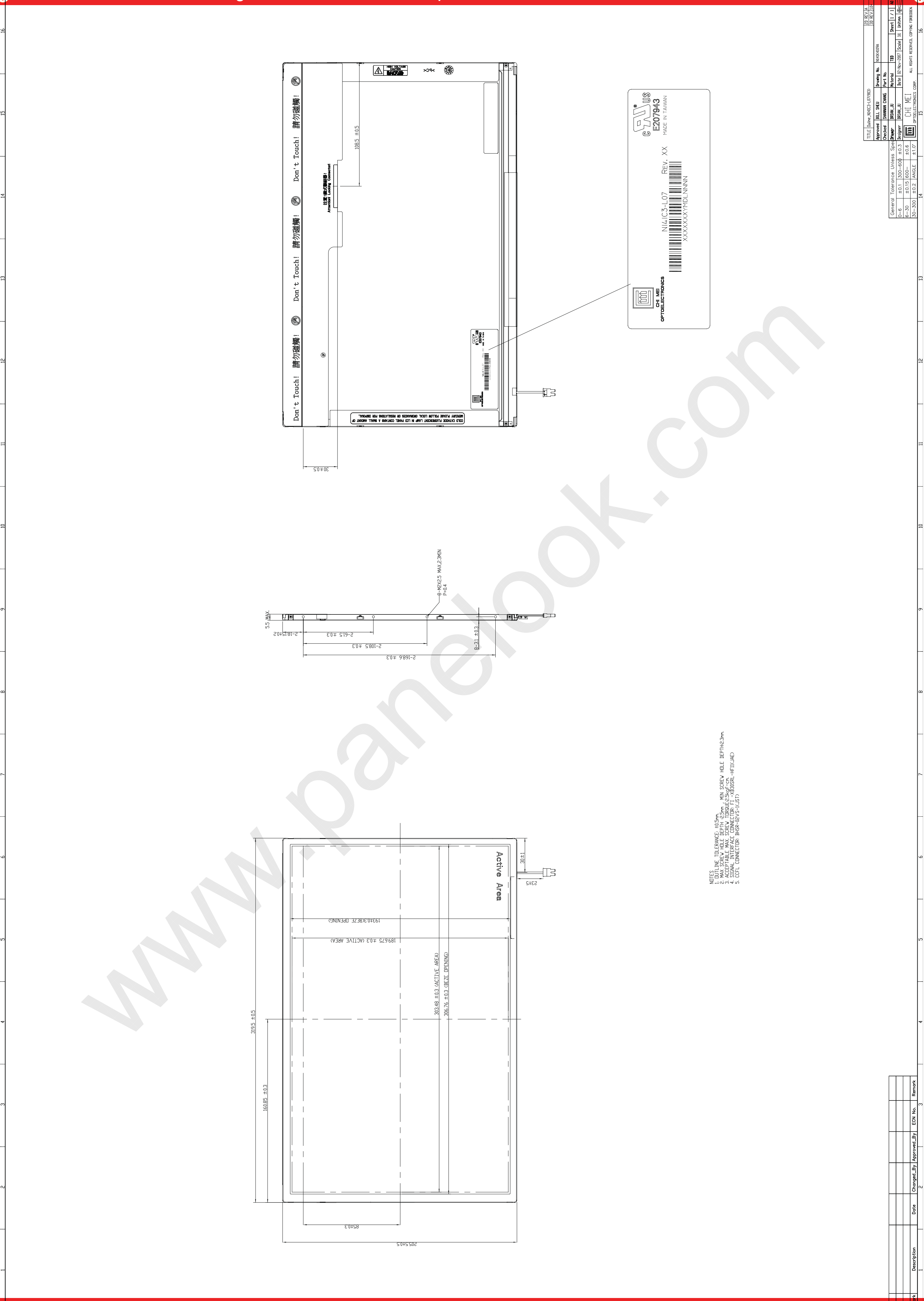
Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

10.2 CMO CARTON LABEL

(a) Production location: Made In XXXX. XXXX stands for production location.



Don't Touch! 請勿碰觸!
Active Area
303.48 ±0.3 (ACTIVE AREA)
306.76 ±0.3 (BEZE OPENING)
189.675 ±0.3 (ACTIVE AREA)
193±0.3(BEZE OPENING)
319.5 ±0.5
205±0.5
160.85 ±0.3
85±0.3
30±0.5
108.5 ±0.5
N141C3-L07
REV. XX
E207943
MADE IN TAIWAN
CHI MEI OPTOELECTRONICS
5.5 MAX.
8-M2X2.5 MAX.2.3MIN P=0.4
NOTES
1. OUTLINE TOLERANCE: ±0.5mm.
2. MAX SCREW HOLE DEPTH :2.5mm , MIN SCREW HOLE DEPTH:2.3mm.
3. ACCEPTABLE MAX. SCREW TORQUE:2.5kgf-cm.
4. SIGNAL INTERFACE CONNECTOR: FI -XB30SRL-HF11(JAE)
5. CCFL CONNECTOR: BHSR-02VS-1(JST)